REMARKS

The above amendments and following remarks are submitted in response to the Official Action of the Examiner mailed November 1, 2002. Having addressed all objections and grounds of rejection, claims 1-20, being all the pending claims, are now deemed in condition for allowance. Reconsideration to that end is respectfully requested.

The Examiner has objected to the specification. In response thereto, Applicants have amended pages 1, 12, and 15 and the abstract. These above amendments as supported by Appendix A are deemed to fully address these objections.

The Examiner has rejected claims 1, 3-5, 7, 8, 13-15, 17 and 20 as containing various informalities. These claims have been amended above in response to these rejections. Support for these amendments are found in Appendix B, hereto attached.

The Examiner has rejected claims 1, 6-7, 11, and 16 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,457,087, issued to Fu (hereinafter referred to as "Fu"). This ground of rejection is respectfully traversed as to the amended claims for the reasons provided below.

"It is axiomatic that for prior art to anticipate under §102 it has to meet every element of the claimed invention, and that such a determination is one of fact". *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81, 90 (Fed. Cir. 1986).

The rejection of claims 1, 6-7, 11, and 16 are respectfully traversed, because the cited prior art does not "meet every element of the claimed invention".

As disclosed and claimed, Applicants' invention is a technique for improving the efficiency of a multiprocessing system employing multiple levels of cache memory coupled to a system memory bus. This enhancement involves providing separate and independent paths to the level two cache and to the tag memories. In that way, SNOOP requests are permitted to directly access the tag memories without reference to the cache memory. A second aspect of the invention, which is not limiting of all pending claims is the establishment of the SNOOP requests at a higher priority than operations associated with local processor data requests, thereby lowering remote processor wait times.

In making his rejection of claims 1 and 6, the Examiner states:

> As per claims 1 and 6, Fu discloses a data processing system having a system bus (i.e., bus 224).....

This finding is clearly erroneous. Bus 224 is "processor bus 224" (see column 7, line 37). The only "system memory bus" to be found in Fu is bus 104 shown in Fig. 1. Fu spends much time distinguishing its approach from that containing a "system bus". It states at column 1, lines 57-59:

> There are several disadvantages with this type of SMW system. The primary disadvantage is the use of the bus as the interconnect structure.

The balance of column 1 through column 2, line 13, details perceived difficulties with the system bus approach. It concludes at column 2, lines 14-15 stating:

> Accordingly, there exists a need for a SMP system that overcomes these shortcomings.

Thus, Fu lists the lack of a "system bus" as one of the important features of its disclosed system.

Though not deemed to change the scope of claims 1 and 6, these claims have been amended to make it absolutely clear that the claimed system memory bus accommodates a plurality of processors. For this reason alone, claims 1 and 6 cannot be found to be anticipated by Fu.

Further in rejecting claims 1 and 6, the Examiner states:

> ....and having a processor with a level one cache memory (i.e., CPU 220 can include a L1 cache) responsively coupled to a level two cache memory....

Whereas column 7, lines 31-34, makes casual reference to an L1 cache memory, there is no teaching or suggestion of its being coupled in any particular manner. Furthermore, there is no evidence within Fu which would establish this as a matter of inherency in accordance with MPEP 2112. Also, the embodiment of Fig. 5C expressly shows L1 cache memory 244 **not** responsively coupled to L2 cache memory 222. On this basis alone, the finding of anticipation by Fu cannot be supported.

In further support of his rejection of claims 1 and 6, the Examiner states:

....and having a circuit for SNOOPing said system bus [col. 16, lines 7-17]....

This finding is clearly erroneous. First, there is no "system bus" in Fu as explained above. Second, the citation (i.e., column 16, lines 7-17) says nothing of SNOOPing processor bus 224 (which the Examiner has found to be the "system bus"). Third, Fu does not SNOOP processor bus 224, because there would be no reason to do so, as processor bus 224 is dedicated to a single processor. The anticipation rejection of claims 1 and 6 is not sustainable in view of this clearly erroneous finding of fact.

In further making his rejection of claims 1 and 6, the Examiner states:

....the improvement comprising a first dedicated path between said system bus and said cache storage (i.e., L2 cache memory 22 has direct path to bus 224)....

Because Fu has no "system bus", it cannot have the claimed path. As explained above, processor bus 224 is not a "system bus". The Examiner makes the same clearly erroneous finding of fact with regard to the "path between said system bus and said tag storage".

Not addressed by the Examiner, claim 6 is further limited by, "A SNOOP request placed on said system memory bus and responsively coupled to said tag memory". Fu does not teach or suggest this claim element.

The Examiner has based his rejection of claims 1 and 6 on quite a number of clearly erroneous findings of fact and has further not shown Fu to contain all of the claimed elements as

required by controlling law. Therefore, the rejection of claims 1 and 6 is respectfully traversed.

In rejecting claim 7, the Examiner states:

> As per claim 7, Fu discloses a data request transferred from said level one cache memory to said level two cache memory [col. 6, lines 38-41].

This finding is clearly erroneous. First, the cited material says nothing of transfers from a level one cache memory to a level two cache memory. In fact, it says nothing of transfers from any particular cache memory to any other particular cache memory. Second, as discussed above, it is not possible to effect the claimed transfer because Fu does not show any level one cache memory coupled to a level two cache memory. Thus, the rejection of claim 7 is respectfully traversed.

Claim 11 is an independent method claim having four individual steps within a particular environment. Even though containing unique limitations, the Examiner has not addressed this environment, but instead refers to his rejection of claim 1. For example, the claim begins "method of maintaining validity of data within a level one cache memory". Fu says nothing of this method (nor was this addressed in the rejection of claim 1).

Furthermore, claim 11 requires "wherein said level two cache memory is responsively coupled to a system memory bus". As explained above, Fu expressly reject the use of a "system memory bus" for his system.

Of the four steps of claim 11, Fu does not have either step b or step c. In finding step b, the Examiner clearly erroneously states:

> ....presenting said SNOOP request on said system memory bus to said level two cache memory (i.e., broadcasting snoop requests to cache lines associated with tag memory 326) [col. 16, lines 11-13]....

Of course, Fu does not have a "system memory bus" on which to present said SNOOP request. Furthermore, the citation says nothing of the SNOOP request being sent to the level two cache memory. Fu does not specify any particular cache level associated with tag memory 326. See Fig. 14 which does not show any cache memory.

In his attempt to find step c, the Examiner states:

> ....routing said SNOOP request directly to said tag memory (tag memory 326 can includes (sic) a set of tags) [col. 16, lines 11-15]....

According to Fu, the SNOOP requests are always routed through "snoop control logic unit 332" rather than directly to the "tag memory" as claimed.

Thus, in rejecting claim 11, the Examiner has missed the entire point of the invention. As explained above, the SNOOP requests are routed directly to the level two cache memory and the level two tag memory through two separate and independent paths. Fu does not have this structure. Furthermore, it would not benefit from this approach because it rejects the technique of a system memory bus which is necessary for and limiting of the claimed invention. The rejection of claim 11 is respectfully traversed.

Claim 16 is an independent apparatus claim containing means-plus-function limitations. The Examiner does not even acknowledge his responsibility in examining this claim in accordance with MPEP 2181, et seq. which describes the controlling law for examination of claim 11. Instead, the Examiner states:

> As per claim 16, Fu discloses the claimed invention as detailed per claims 1 and 11 above....

It is Applicants' position that the Examiner's statement of itself renders the examination defective as a matter of law.

The Examiner further states:

> Fu further discloses caching data in the next level when said data does not reside at the lower level cache [col. 6, lines 38-48].

This statement is both clearly erroneous factually and irrelevant as a matter of law. The statement is clearly erroneous because the citation says nothing of transfers from one cache memory to another. In addition, there is certainly no "requesting means" as is limiting of element c.

The statement is also legally irrelevant because it looks to Fu rather than Applicants' specification for structural support of the claimed "means". Therefore, even if the statement of the Examiner were not clearly erroneous, it would have nothing to do with establishment of anticipation as required by MPEP 2181 et seq.

The Examiner has rejected claims 2-4, 8-10, 12-13[1], and 17-20 under 35 U.S.C. 103(a) as being unpatentable over Fu in view of U.S. Patent No. 6,457,087, issued to Stevens et al (hereinafter referred to as "Stevens"). This ground of rejection is respectfully traversed as to the amended claims for the following reasons.

MPEP 2143 defines the required showings for the Examiner to present a *prima facie* case of obviousness. To paraphrase, the Examiner is required to show: 1)motivation to make the alleged combination; 2)reasonable likelihood of success of the alleged combination; and 3)all claimed elements present within the alleged combination. The rejections of claims 2-4, 8-10, 12-15, and 17-20, as amended, are respectfully traversed for failure of the Examiner to make a *prima facie* case of obviousness as required by MPEP 2143.

The Examiner rejects claims 2, 12, and 17 as if they all had the same scope. Each of these has a separate legal basis of patentability and different standard for examination. Claim 2 is an apparatus claim; claim 12 is a method claim; and claim 17 contains means-plus-function limitations. Therefore, the Examiner's rejection is procedurally incorrect, as a matter of law.

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[1]Apparently the Examiner intended to include claims 14 and 15 in this rejection, as he discusses claims 14-15 separately.

The Examiner goes on to admit that Fu does not teach a control logic which provides the highest priority for a SNOOP function. He then states:

> Stevens et al. disclose the concept of a control logic which provides the highest priority for a SNOOPing [col. 4, lines 23-32]

This is legally irrelevant because it doesn't address the limitations of the claim sought to be rejected. Instead, the Examiner says that Stevens discloses "the concept....". There is no showing in the citation of the structural elements to which the alleged "control logic" is coupled, as required by claim 2. There is no data request step from a level one cache memory, as required by claim 12. There is showing in the citation of the coupling required of claim 17. Thus, the Examiner has not even stated that the alleged combination has all of the claimed elements of claims 2, 12, and 17. Furthermore, he could not do so without making a clearly erroneous finding of fact. Therefore, the Examiner has failed to so all claimed elements within the alleged combination.

In an attempt to show motivation for the alleged combination, the Examiner states:

> It would have been obvious to one of ordinary skill in the art, having the teachings of Fu and Stevens et al. before him at the time the invention was made, to modify the system of Fu to include a control logic which provides the highest priority for a SNOOPing because it would have provided minimal effect on system speed by allowing the cache system to efficiently service its local processor while also guaranteeing access to all snoop requests on the <u>host bus</u> to maintain cache

> coherency [col. 4, lines 15-20] as taught b y Stevens et al. (emphasis added)

The most apparent reason why this statement is false on its face is that Fu has no host bus. Fu specifically teaches against such an architecture, as discussed above. Therefore, the Examiner has not shown motivation for the alleged combination.

The Examiner does not even address the requirement that he show reasonable likelihood of success of the alleged combination. Thus, the rejection of claims 2, 12, and 17 is respectfully traversed for failure of the Examiner to make any of the three showings required by MPEP 2143.

Claim 3 depends from claim 2 and further limits the level two cache memory to include a "duplicate tag memory". The Examiner states:

> AS per claim 3, Fu discloses a level two cache memory further comprising a duplicate tag memory (i.e., L2 duplicate tag memory 234) [Fig. 5A].

This statement is clearly erroneous. Duplicate tag memory 234 is located within and is a portion of FCU 212. It is expressly not located within nor a portion of L2 cache memory 222. The rejection of claim 3 is respectfully traversed for failure of the Examiner to present any of the three showings required by MPEP 2143.

Claim 4, as amended, requires that the plurality of instruction processors be coupled by a "system memory bus". As explained above, Fu disclaims the use of any system memory bus. The rejection of claim 4 is respectfully traversed for failure of

the Examiner to present any of the three showings required by MPEP 2143.

The Examiner rejects claims 9, 13, and 19 with the same broad brush. As explained above, this approach is not in accordance with controlling law which holds different examination standards for these diverse claims. The rejection of claims 9, 13, and 19 is respectfully traversed at least for this reason.

The Examiner continues his rejection of claims 9, 13, and 19 by citing portions of Figs. 5A and 5C. However, Fu clearly states at column 3, lines 28-33, that Fig. 5A and Fig. 5C discloses different and alternative embodiments of Fu's invention. Thus, it is at least disingenuous for the Examiner to suggest that the components of Fig. 5A and the components of Fig. 5C are somehow complimentary rather than being mutually exclusive as disclosed by the reference itself.

Furthermore, the Examiner does not address the actual claim elements of claims 9, 13, and 19 rendering his rejection legally irrelevant. In addition, the Examiner is clearly erroneous in stating:

> ....a duplicate tag memory which maintains a duplicate of information within said level one tag memory (i.e., L2 duplicate tag memory 234) [Fig. 5A]

Though Fig. 5A shows Duplicate L2 Tag Memory 234, it clearly shows it located in and as a portion of FCU 212. It says nothing of whether it "maintains a duplicate of information within said level

one tag memory". Therefore, the rejection of claims 9, 13, and 19 is respectfully traversed as based upon clearly erroneous findings of fact and incorrect application of both procedural and substantive controlling law.

The Examiner attempts to reject both claim 10 and claim 20 by addressing only the limitations of claim 10. Thus, the rejection of claim 20 is respectfully traversed as not having been addressed by the Examiner. He has not even attempted to present a *prima facie* case of obviousness as required by MPEP 2143.

In rejecting claim 10, the Examiner states:

> Fu discloses a data processing system wherein a snoop request is responsively coupled to said duplicate tag memory [col. 15, 48-51, col. 16, 7-8]. (emphasis added)

This is finding is clearly erroneous. The citation says at column 16, lines 7-8:

> The snoop control logic unit 332 is coupled to the tag memory 326....

Thus, it is clear that in Fu, the coupling is to the "tag memory" and not a "duplicate tag memory" as is limiting of the claim. Therefore, the rejection of claim 10 is respectfully traversed.

In rejecting claim 14, the Examiner states:

> ....[tag memory 326 can include duplicate tags] [col. 16, lines 11-15].

The citation provided says nothing of "duplicate tags". Therefore, it is apparent that the Examiner has either made a clearly erroneous finding of fact by misreading the reference, or has made

a finding of fact without any supporting authority. In either case, the rejection of claim 14 is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as required by MPEP 2143.

The Examiner has created a similar situation with regard to his rejection of claim 15. The citation does not mention "duplicate tag memory" at all. The rejection of claim 15 is respectfully traversed.

Claim 18 depends from claim 17 and is further limited by "means for bussing system data". As explained above, Fu takes great pride in not using any system bus within his system. The "processor bus 224" is not a "means for bussing system data" for the reasons stated above. Furthermore, MPEP 2181 requires that the Examiner construe "means for bussing system data" in view of Applicants' specification and drawings. For both reasons, Fu does not teach or suggest the claim limitation. Therefore, the rejection of claim 18 is respectfully traversed.

The Examiner has rejected claim 5 as being unpatentable over Fu in view of Stevens and further in view of U.S. Patent No. 6,353,877, issued to Duncan et al (hereinafter referred to as "Duncan"). This rejection is respectfully traversed for failure of the Examiner to provide a *prima facie* case of obviousness.

The Examiner admits that neither Fu nor Stevens nor the combination thereof shows the claimed limitations. Therefore, he alleges motivation to combine Duncan stating:

> ....because it would have provided higher processor performance by reducing the period of time that the processor must wait to retrieve data and instructions from the main memory by temporarily storing large portions of data in the third level cache [col. 6, lines 32-35] as taught by Duncan.

The higher processor performance claimed in Duncan is based on a bussed architecture. Column 4, lines 21-23, of Duncan states:

> Referring now to FIG. 1, a multi-processor computer system **10** is shown to include a plurality of Central Processor Units (CPU) **12-18** coupled together via a system bus **20**.

Thus, it is readily apparent that an adherent of Fu would not be likely to combine the teachings of Duncan, because of Fu's aversion to a bussed system architecture. Furthermore, even if one were to attempt the alleged combination, there would be no improvement in efficiency unless one were to build Fu around a system bus, which would render Fu inoperative.

Therefore, the rejection of claim 5 is respectfully traversed for failure of the Examiner to have make the three showings required of MPEP 2143.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-20, being the only pending claims.

Respectfully submitted,

Donald C. Englin et al.

By their attorney,

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Lawrence M. Nawrocki
Reg. No. 29,333
Suite 401
Broadway Place East
3433 Broadway Street N.E.
Minneapolis, Minnesota
55413
(612) 331-1464

APPENDIX A (Support for Specification Amendments)

Please amendment the specification as follows:

1. In the Abstract, line 8, replace "give" with -given--;

2. At page 1, line 6, replace "_____, filed _____" with -09/626,030, filed July 27, 2000-;

3. At page 1, line 9, replace "_____, filed _____" with -08/650,800, filed August 30, 2000-;

4. At page 1, line 11, replace "_____, filed _____" with -09/650,730, filed August 30 2000-;

5. At page 1, lines 12-13, replace "_____, filed _____" with -08/235,196, filed April 29, 1994-;

6. At page 12, line 16, replace "data path logic 70" with -data path logic 68-; and

7. At page 15, line 5, replace "write" with -right-.

Appendix B (Support for Claim Amendments)

1. (First Amended) In a data processing system having a plurality of processors coupled via a system memory bus and having a first processor of said plurality of processors with a level one cache memory responsively coupled to a level two cache memory which is responsively coupled to a level three memory, said level two cache memory having cache storage and tag storage and having a circuit for SNOOPing said system memory bus, the improvement comprising:

[a.] A first dedicated path between said system memory bus and said cache storage and a second dedicated path between said system memory bus and said tag storage.

2. (Unchanged) A data processing system according to claim 1 further comprising control logic responsively coupled to said cache storage and said tag storage which provides the highest priority for said SNOOPing.

3. (First Amended) A data processing system according to claim 2 wherein said level two cache memory further comprises:

[a.] A duplicate tag memory.

4. (First Amended) A data processing system according to claim 3 wherein said plurality of processors further [comprising:] comprises

[a.] A plurality of instruction processors.

5. (First Amended) A data processing system according to claim 4 wherein said level three memory further comprises:

[a.] A level three cache memory.

6. (First Amended) A data processing system comprising:

a. A plurality of processors including a first processor having a level one cache memory;

b. A level two cache memory having a data memory and a tag memory responsively coupled to said level one cache memory;

c. A system memory bus responsively coupled to said plurality of processors and responsively coupled to said data memory and responsively coupled to said tag memory; and

d. A SNOOP request placed on said system memory bus and responsively coupled to said tag memory.

7. (First Amended) A data processing system according to claim 6 further comprising:

[a.] A data request transferred from said level one cache memory to said level two cache memory.

8. (First Amended) A data processing system according to claim 7 further comprising:

[a.] Control logic within said level two cache memory which provides priority of said SNOOP request over said data request.

9. (First Amended) A data processing system according to claim 8 further comprising:

a. A level one tag memory located within said level one cache memory; and

b. A duplicate tag memory within said level two cache memory which maintains a duplicate of information within said level one tag memory.

10. (First Amended) A data processing system according to claim 9 wherein said SNOOP request is responsively coupled to said duplicate tag memory.

11. (Unchanged) A method of maintaining validity of data within a level one cache memory of a processor having a level one tag memory responsively coupled to a level two cache memory having

a tag memory and a data memory wherein said level two cache memory is responsively coupled to a system memory bus comprising:

a. Formulating a SNOOP request;

b. Presenting said SNOOP request on said system memory bus to said level two cache memory;

c. Routing said SNOOP request directly to said tag memory; and

d. Processing said SNOOP request.

12. (Unchanged) A method according to claim 11 further comprising:

a. Presenting a data request from said level one cache memory to said level two cache memory; and

b. Granting priority to said SNOOP request over said data request.

13. (First Amended) A method according to claim 12 further comprising:

[a.] Maintaining a duplicate copy of said level one tag memory within a duplicate tag memory within said level two cache memory.

14. (First Amended) A method according to claim 13 further comprising:

[a.] Routing said SNOOP request to said duplicate tag memory.

15. (First Amended) A method according to claim 14 further comprising:

[a.] Processing said SNOOP request regarding said duplicate tag memory.

16. (First Amended) An apparatus comprising:

a. Means for executing program instructions;

b. Means responsively coupled to said executing means for level one caching data;

c. Means responsively coupled to said executing means and said level one caching means for requesting a data element if said executing means requires requesting of said data element and said level one caching means does not contain said data element;

d. Means responsively coupled to said requesting means for level two caching;

e. Means located within said level two caching means for storing level two caching data;

f. Means located within said level two caching means for maintaining level two tags; and

g. Means responsively coupled to said maintaining means for directly SNOOPing said level two [tag1] <u>tags</u>.

17. (Unchanged) An apparatus according to claim 16 further comprising:

a. Means responsively coupled to said storing means and said maintaining means for granting priority to a SNOOP request over said data element request.

18. (Unchanged) An apparatus according to claim 17 further comprising:

a. Means responsively coupled to said level two caching means for bussing system memory data;

b. Means responsively coupled to said bussing means for interfacing said bussing means directly to said storing means; and

c. Means responsively coupled to said bussing means for interfacing said bussing means directly to said maintaining means.

19. (Unchanged) An apparatus according to claim 18 further comprising:

a. Means located within said level one caching means for recording level one tags; and

b. Means located within said level two caching means and responsively coupled to said recording means for duplicating said level one tags.

20. (Unchanged) An apparatus according to claim 16 further comprising:

a. Means responsively coupled to said bussing means and said duplicating means for SNOOPing said duplicating means.